RECEIVED
CENTRAL FAX CENTER
NOV 15 2006

REMARKS

The Office Action of 08/15/2006 has been carefully considered. Reconsideration in view of the present remarks is respectfully requested.

Claims 1-10 were rejected as being unpatentable over Ishida in view of Tomita et al. The rejection states in part:

> [I]shida discloses a static semiconductor device...arranged to reduce write strengths required to write data into individual ones of the memory cells...*relative to a drive strength of the bit line circuits*.

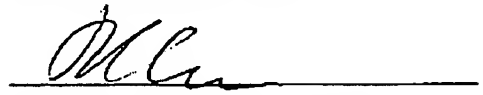
This rejection is respectfully traversed.

Ishida is silent concerning drive strengths required to write data into individual ones of the memory cells, relative to a drive strength of the bit line circuits. Figure 9 of Ishida shows a memory cell 3a including two inverters. Input signals to the inverters are provided by the bit lines. *However, nowhere does Ishida discuss or show the supply voltages of the inverters.* It is the supply voltages of the inverters relative to the bit line voltages that determine the drive strength to write data into individual ones of the memory cells. Note for example Figure 2 of the present application and accompanying description (pages 6 and 7).

Ishida merely discloses circuitry for reducing the bit line voltage compared to the supply voltage Vcc.

Withdrawal of the rejection and allowance of claims 1-10 is respectfully requested.

Respectfully submitted,



Michael J. Ure, Reg. 33,089

Dated: 11/13/06